Journal of Power Sources 198 (2012) 312–317

Contents lists available at SciVerse ScienceDirect

Journal of Power Sources

journal homepage: www.elsevier.com/locate/jpowsour

Short communication

Self-aligned Cu–Si core–shell nanowire array as a high-performance anode for Li-ion batteries

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ARTICLE INFO

Article history:
Received 18 July 2011
Received in revised form
30 September 2011
Accepted 3 October 2011
Available online 8 October 2011

Keywords:
Lithium-ion
Anode
Copper
Silicon
Core–shell
Nanowires

ABSTRACT

Silicon nanowires (NWs) have been reported as a promising anode that demonstrated high capacity without pulverization during cycling, however, they present some technical issues that remain to be solved. The high aspect ratio of the NWs and their small contact areas with the current collector cause high electrical resistance, which results in inefficient electron transport. The nano-size interface between a NW and the substrate experiences high shear stress during lithiation, causing the wire to separate from the current collector. In addition, most reported methods for producing silicon NWs involve high-temperature processing and require catalysts that later become contaminants. This study developed a new self-aligned Cu–Si core–shell NW array using a low-temperature, catalyst-free process to address the issues described. The silicon shell is amorphous as synthesized and accommodates Li-ions without phase transformation. The copper core functions as a built-in current collector to provide very short (nm) electron transport pathways as well as backbone to improve mechanical strength. Initial electrochemical evaluation has demonstrated good capacity retention and high Coulombic efficiency for this new anode material in a half-cell configuration. No wire fracture or core–shell separation was observed after cycling. However, electrolyte decomposition products largely covered the top surface of the NW array, restricting electrolyte access and causing capacity reduction at high charging rates.

1. Introduction

The graphite anode currently used for Li-ion batteries has a relatively low theoretical capacity, 372 mAh g^{-1}. Among known candidate anode materials, silicon has the highest theoretical charge capacity (4200 mAh g^{-1}) [1]. However, silicon experiences a huge volume expansion (up to 400%) upon insertion of Li^+ during charging, each Si atom alloying with an average of 4.4 Li atoms. The enormous stresses thus generated make silicon anodes in bulk [1] or thin film [2] forms vulnerable to pulverization leading to rapid capacity fade during cycling.

Attempts have been made to deal with the durability of silicon anodes using various nanostructures, such as carbon-coated silicon nanoparticles [3], nanocomposites incorporated with carbon nanotubes [4], nanoporous silicon [5], silicon nanotubes [6], and silicon nanowires (NWs) [7,8]. Specifically, Cui's group [7] recently reported that silicon NWs can accommodate the large strain from Li^+ insertion without pulverization. However, the electron transport paths inside a silicon NW, in the longitudinal direction, have relatively high electrical resistivity because of the high aspect ratio (length on the scale of μm and diameter in the scale of tens of nm), as illustrated in Fig. 1a. The nano-size interface between a NW and the current collector results in a high electrical contact resistance, which also impairs the efficiency of electron transport. In addition, the small contact area undergoes a high shear stress when silicon swells during lithiation, potentially causing wire separation from the substrate (Fig. 1a).

Here we propose a self-aligned metal–silicon core–shell NW array as a potential high-performance anode material [9]. The silicon shell provides high capacity while the metal core functions as a built-in current collector and enhances the NW strength and toughness. As shown in Fig. 1b, the metal core shortens the electron transport path from micrometers (longitudinal axis) to nanometers (radial axis) scale. The core–shell structure ensures a large contact area between silicon (shell) and current collector (core), and thus a low contact resistance. The metal core is directly rooted on the current collector and maintains a reliable connection both mechanically and electronically. The self-aligned nanostructure avoids wire interlock-induced stress concentration

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doi:10.1016/j.jpowsour.2011.10.004

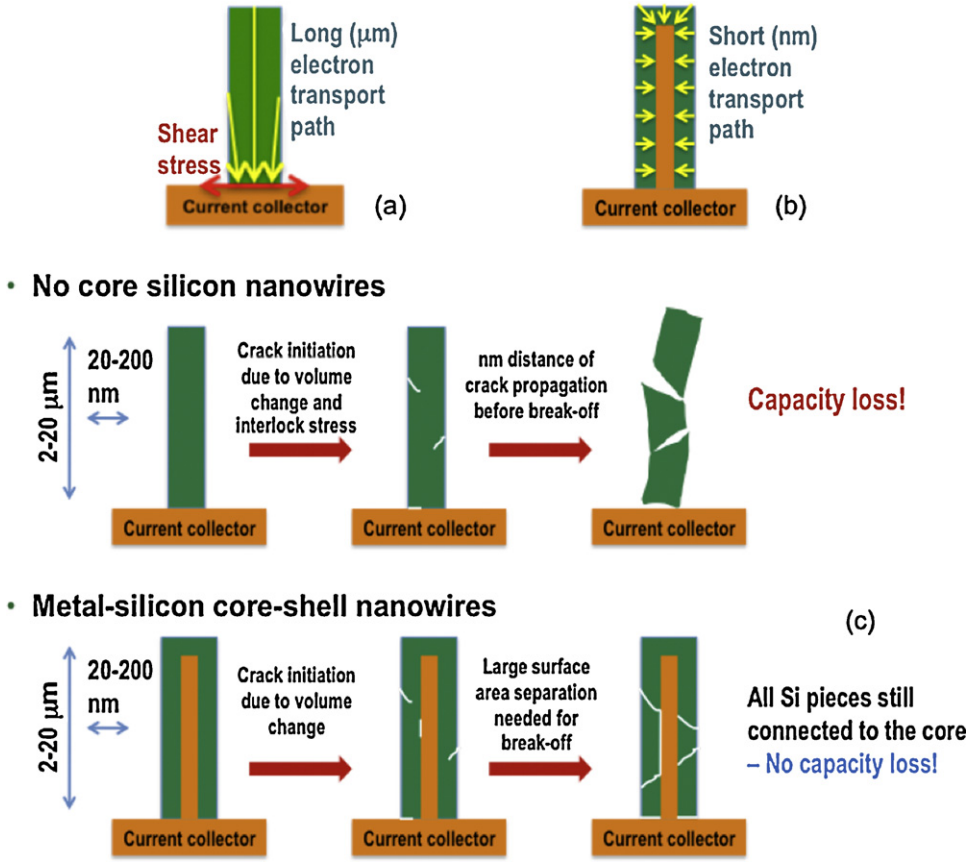

Fig. 1. Schematic of wires with added metal cores to improve the electrical and mechanical properties of silicon NWs. (a) A no-core silicon NW having a long (μm) electron transport path and high shear stress at the interface with the current collector during charging/discharging. (b) A metal–Si core–shell NW having a short (nm) electron transport path and no shear stress between the metal core and the current collector. (c) The metal core substantially improves the fracture toughness of the NW.

during charging. Although the NW geometry is proven to sustain large volume change, cracking still may occur during cycling as a result of the brittle nature of silicon and inevitable nanostructure defects or composition contaminants. In a conventional silicon NW without a core, a crack, once initiated, would easily propagate in the radial direction (nm path) to break the wire (Fig. 1c). In contrast, a metal core would either stop a crack or force it to propagate in the longitudinal direction (μm path), as illustrated in Fig. 1c. For a cracked core–shell NW, as long as each silicon piece still contacts the metal core, there is no capacity loss. Compared with the previously reported Si(crystalline)–Si(amorphous) [10], C-Si [11], and Si-C [12] core–shell NWs, this Cu–Si core–shell NW array has potential advantages including more ordered structure, higher mechanical strength, and improved electrical conductivity.

In addition to their potentially superior anode performance, the production of such metal–silicon core–shell NW arrays is low-cost and scalable. Unlike conventional techniques for fabricating silicon-based NWs that require high temperature and catalysts, such as vapor–liquid–solid (VLS) and pulsed-laser deposition (PLD), the synthesis of metal–silicon core–shell NWs in this study is based on a hybrid process involving wet chemical electrodeposition and plasma-enhanced chemical vapor deposition (PECVD) at modest temperatures.

2. Experimental

In this proof-of-concept study, copper was chosen as the core material and a Cu–Si core–shell NW array was synthesized using the procedure illustrated in Fig. 2. Similar to the approach described in [13,14], template-aided electrodeposition was used to grow copper NWs (see Figs. 2a–c). The nanoporous template was a 6-μm thick track-etched polycarbonate (PC) membrane. The nanopores have a nominal diameter of 100 nm and a pore density of 4×10^8 cm^{-2}. A thin gold film (~100 nm) was first sputtered on the backside of the PC membrane by metal evaporation. This gold layer is too thin to fully cover the pores. A thicker copper backplate (>10 μm) was then electrodeposited on top of the gold film in an aqueous solution containing 0.6 M $CuSO_4$ and 1.0 M H_2SO_4. The deposition was conducted using a three-electrode configuration on a CHI model 660A potentiostat/galvanostat (CH Instruments, Austin, TX). The counter electrode was platinum and the reference electrode was Ag/AgCl. Electrodeposition was carried out at potential of −0.4 V for 1 h. The copper backplate effectively sealed the bottoms of the nanopores and functioned as the electrode in the next step. As shown in Fig. 2b, copper NWs grew on the copper backplate and filled the volume of the nanopores. An electrodeposition configuration and parameters similar to those used to deposit the copper backplate were used to grow the copper NWs. After a relatively short deposition time (~10 min), copper NWs started growing out of the top surface of the template and forming mushroom heads. A sudden increase in the deposition current usually indicated such a phenomenon and was used to signal the point at which to terminate the deposition. The PC membrane was then etched off in CH_2Cl_2, as illustrated in Fig. 2c, to expose the self-aligned copper NW array.

In the final step shown in Fig. 2d, a silicon layer was deposited on the copper NWs via PECVD. Thanks to the fast development of photovoltaic (PV) thin film technology [15], PECVD for depositing silicon thin films at relatively low process temperatures has been well developed [16]. The PECVD was conducted at 250 °C

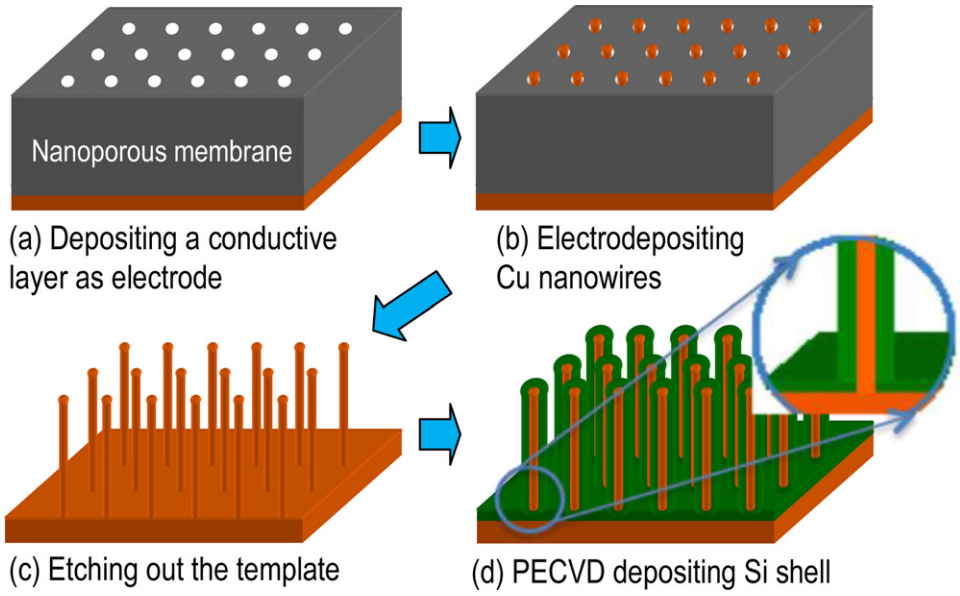

Fig. 2. Schematic of the processes for synthesizing a self-aligned metal–silicon core–shell NW array (Color scheme: grey: nanoporous template; gold: copper; and green: silicon). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of the article.)

using a 40 Ws DC plasma for 7 h and 15 min in a custom-built CVD system. The feedstock silane was supplied at a constant rate of 15 $cm^3\ min^{-1}$ along with argon at 50 $cm^3\ min^{-1}$ and the chamber pressure was maintained at 10.4 Torr.

A two-electrode coin-type half-cell was assembled for the Cu–Si NW array with a lithium metal foil as the counter electrode. This half cell had a polypropylene membrane separator (Celgard, Inc.) and standard electrolyte (Novolyte Technologies) composed of 1.2 M $LiPF_6$ in a blend of ethylene carbonate (EC) and dimethyl carbonate (DMC) in a 1:2 weight ratio. The cell was assembled in a glove box purged with high-purity argon. Galvanostatic charge–discharge cycling was carried out using a multichannel battery tester (Maccor, Inc., model 4000). Tests were conducted in a potential range of 2.0–0.005 V using a constant current charge–discharge protocol at rates varying from C/30 to 10C. The currents were calculated using the actual capacity measured in the first cycle, e.g., the current at 1C was0.27 mA cm^{-2}.

The morphology and chemical composition of the copper NW array and the Cu–Si core–shell NW array before and after cycling were examined and analyzed using scanning electron microscopy (SEM) along with energy-dispersive X-ray spectroscopy (EDS) on a Hitachi FE-SEM S4800 as well as transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS) on an aberration-corrected FEI Titan S 80-300 TEM/STEM equipped with a Gatan Image Filter Quantum-865. Raman spectra were collected from the Cu and Cu–Si NW using a Dilor XY800 Microprobe (JY Inc., Edison, NJ) with an Innova 308c Ar^+ laser (Coherent, Inc., Santa Clara, CA) operating at 5145 Å in order to identify crystalline and amorphous silicon phases and to detect silicon oxides if any were present.

3. Results and discussion

The SEM image in Fig. 3a shows a copper NW array produced using the procedure illustrated in Figs. 2a–c. The NWs are a relatively uniform size with fairly good alignment. The wire length is in the range of 4–6 μm. It was interesting to observe that the wire diameter of ~180 nm is much larger than the nominal pore size (~100 nm) in the PC membrane. This is probably because the deformability of polycarbonate allowed pore expansion during the copper wire growth.

The Cu–Si core–shell NW array after silicon coating is shown in Fig. 3b. All copper NWs are well covered with a silicon shell. The outer diameter is ~300 nm at the wire tip and ~220 nm near the root. This indicates a thicker (~60 nm) silicon layer at the wire top portion and a thinner (~20 nm) silicon layer at the wire bottom portion. The TEM imaging and EELS element mapping of a wire bottom segment are shown in Fig. 3c and d, respectively, which confirm the Cu–Si core–shell structure.

The EDS examination from the top of the NW array confirmed existence of the silicon layer and implied the Cu and Si contents of 61.2 and 33.4 wt.% (Fig. 3e), which matched well with the calculated values (68 and 32 wt.%) for the top portion of a NW based on wire dimensions. The oxygen content (5.1 wt.%) suggested that the NWs were slightly oxidized. Raman spectra from both the Cu and Cu–Si NW arrays are shown in Fig. 3f. Metallic Cu has no Raman features and the weak peaks are due to the background of the instrument. The Cu–Si NW array exhibited a broad peak centered at 485 cm^{-1} that is associated with amorphous Si [17–19] and a sharp peak at 520 cm^{-1} that is the well-known crystalline Si peak. The amorphous phase appears to dominate the Si shell based on its intensity and peak area relative to the crystalline phase. Amorphous silicon is preferred over crystalline silicon for the anode application because it does not undergo phase transformation and tends to expand isotropically upon Li-ion insertion [20].

The theoretical charge capacity for a Cu–Si core–shell NW array can be calculated using the following formula with respect to unit mass (C_{NWs_W}), volume (C_{NWs_V}), and area (C_{NWs_A}).

$$C_{NWs_W\left(\frac{mAh}{g}\right)} = \frac{\rho Si \cdot (D^2 - d^2) \cdot C_{Si}}{\rho Si \cdot (D^2 - d^2) + \rho_{Cu} \cdot d^2} \quad (1)$$

$$C_{NWs_V\left(\frac{mAh}{cm^3}\right)} = \rho Si \cdot \pi \frac{(D^2 - d^2)}{4} \cdot \eta_{wire\text{-}density} \cdot C_{Si} \quad (2)$$

$$C_{NWs_A\left(\frac{mAh}{cm^2}\right)} = \rho Si \cdot \pi \frac{(D^2 - d^2)}{4} L \cdot \eta_{wire\text{-}density} \cdot C_{Si} \quad (3)$$

where C_{Si}: capacity of silicon; ρ_{Si}: density of silicon; ρ_{Cu}: density of copper; D: diameter of the silicon shell; d: diameter of the copper core; $\eta_{wire\text{-}density}$: number of NWs per unit area; L: length of NWs.

The calculated charge capacity for this particular Cu–Si NW array in Fig. 3b is ~883 mAh g^{-1} (corresponding to the variation

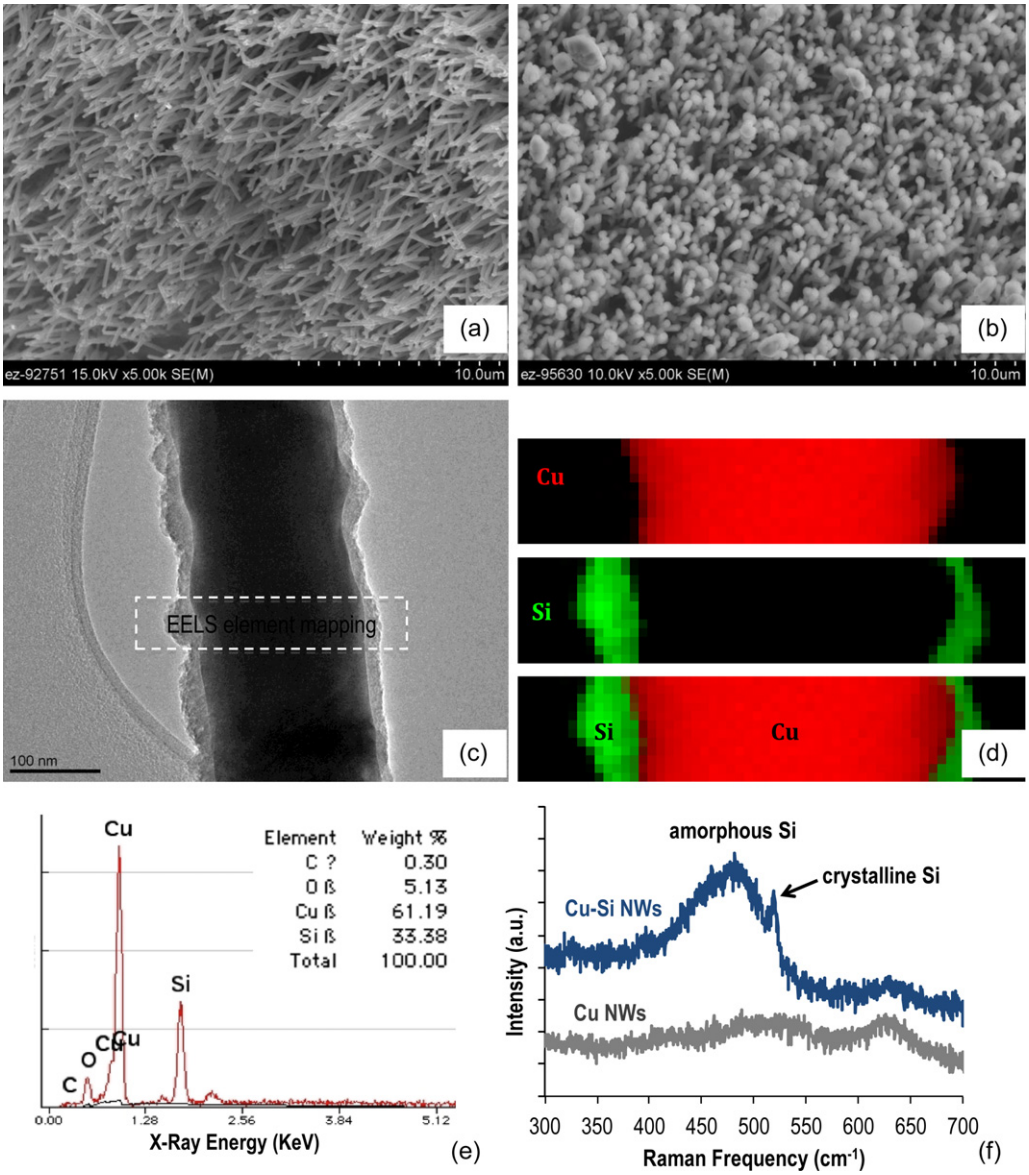

Fig. 3. (a) SEM image of the Cu NW array produced by template-aided electrodeposition; (b) SEM image of the NW array after Si deposition via PECVD; (c) TEM image and (d) EELS element maps of a NW bottom segment confirming the Cu–Si core–shell structure; (e) EDS examination from the NW array top; and (f) Raman spectrum suggesting the Si shell dominated by amorphous phase.

in NW core and shell diameters) using Eq. (1), assuming the theoretical capacity of 4200 mAh g^{-1} for silicon. If each nanopore in the PC membrane produces a NW (wire density = pore density = 4×10^8 cm^{-2}), the volumetric capacity can be computed using Eq. (2) to be ~1082 mAh cm^{-3}. Considering the wire length of 4–6 μm, the unit area capacity was estimated to be ~0.54 mAh cm^{-2} according to Eq. (3).

The half-cell testing results are shown in Fig. 4. The 1st lithiation under the C/30 charge rate indicated a capacity of 0.27 mAh cm^{-2}, which is only half of the calculated capacity. Possible reasons include: (1) the actual capacity of the silicon may be lower than 4200 mAh g^{-1} and a small portion of the silicon shell was oxidized, and (2) the number of functional NWs is less than the number of pores in the template (some pores failed to produced NWs and some NWs were broken during the synthesis process or cell assembly). The first cycle Coulombic efficiency was 63%. Although, the exact mechanism for the irreversible capacity loss in the 1st cycle is unclear, solid electrolyte interphase (SEI) layer formation [21] may play an important role due to the large silicon surface area of the NW array. In addition, the lithium ions consumed by SiO_x ($SiO_x + 2Li \rightarrow Si + xLi_2O$) in the silicon shell was non-releasable, which also contributed to the low Coulombic efficiency in the first cycle.

The Coulombic efficiency went up to 100% in the second cycle and subsequently remained in a narrow range of 97–100% afterward. The charge capacity stabilized at ~0.17 mAh cm^{-2} at the C/30 cycling rate after the first cycle. From cycle #3 to cycle #26 when the cycling rate increased from C/30 to 2C, the measured capacity gradually decreased to 0.12 mAh cm^{-2}. However, the capacity degradation accelerated significantly at 5C and 10C. By the end of the last cycle (#36) at 10C, the capacity had dropped to ~0.02 mAh cm^{-2}. There are two possibilities for the dramatic capacity reduction: either a permanent capacity loss due to wire damage or restricted charge transport at high charging rates. To identify the cause, C/10 was used again in the cycles #37–39 and the capacity was immediately restored to 0.16 mAh cm^{-2}, which is ~95% of the capacity at C/10 tested in the early cycles #4–8. This indicates that the permanent capacity loss was minimal if any.

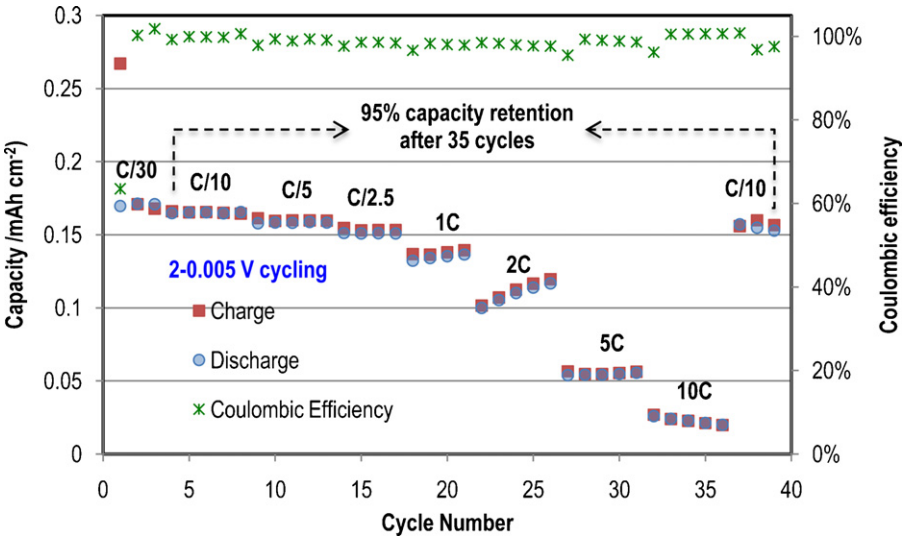

Fig. 4. Charge–discharge cycling performance of a Cu–Si NW array as the anode in half-cell testing.

The cell was dissembled after 39 testing cycles and the morphology and chemical composition of the cycled Cu–Si core–shell NW array were then examined. The top-view and side-view SEM images in Fig. 5a and b clearly reveal a 3–4 μm thick layer largely covering the top surface of the NW array. EDS analysis detected high concentrations of oxygen (43 at.%), carbon (27 at.%), and fluorine (10 at.%) in this layer, as shown in Fig. 5c. This suggests that this layer is primarily composed of decomposition products of the electrolyte. The exact cause of such severe electrolyte decomposition is not yet known, and it requires further investigation. Nevertheless, this layer restricted the electrolyte access to the NWs, contributing to the reduced capacity at fast cycling rates (see Fig. 4).

Despite the unexpected electrolyte decomposition layer on the top, the Cu–Si core–shell NWs themselves remain intact without apparent wire pull-out, silicon pulverization, or core–shell delamination after 39 cycles of lithiation and delithiation (see Fig. 5b).

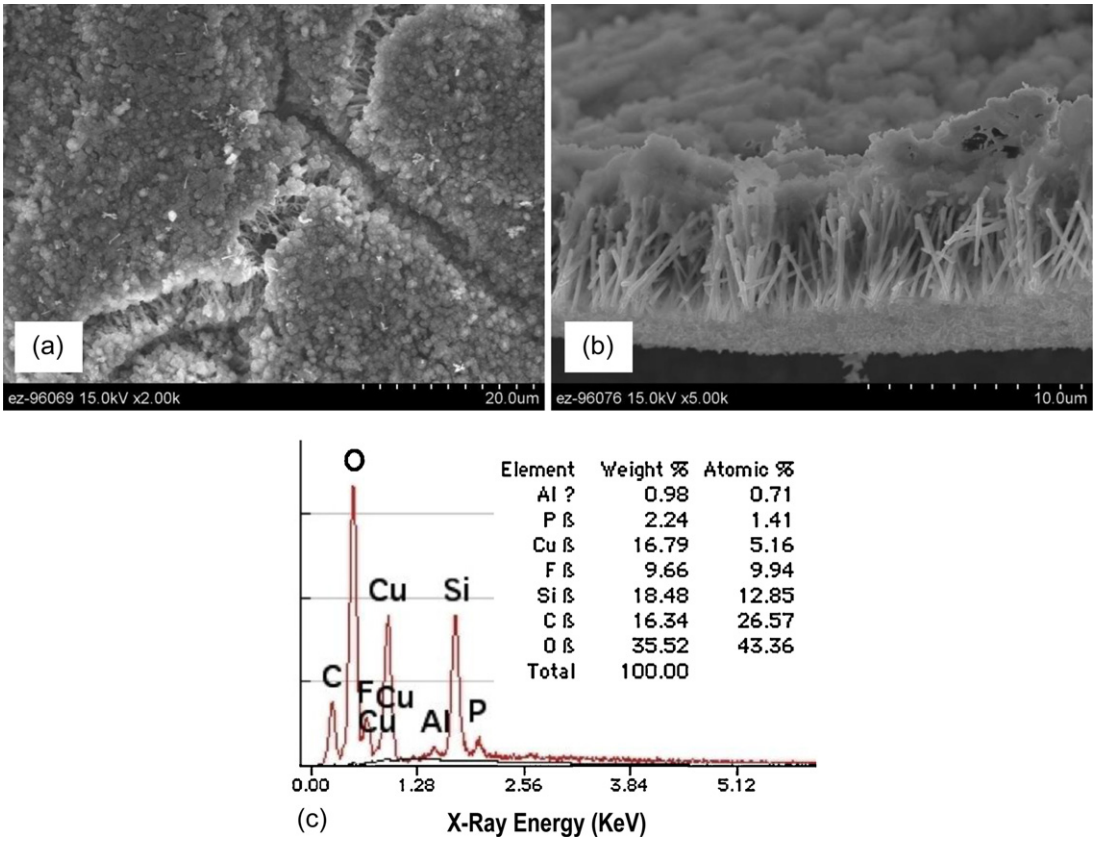

Fig. 5. A layer of electrolyte decomposition products covering the top surface of the Cu–Si NW array, restricting the electrolyte access and thus causing low capacity at fast cycling: (a) SEM top view, (b) SEM side view, and (c) EDS spectrum.

Results of this study demonstrated the feasibility of the synthesis process for the Cu–Si core–shell NW array and its application as an anode. Further research and development are needed to explore and realize the full potential of this unique nanostructured material. For instance, unit mass capacity above 3000 mAh g^{-1} is possible with a thicker silicon layer and/or a thinner copper core. In addition to increasing the Si:Cu ratio, using a template with higher pore density and growing longer NWs may generate an areal capacity as high as 5 mAh cm^{-2}. The irreversible capacity loss seen in the first cycle may be reduced by controlling the SEI formation and limiting the silicon oxide formation. The electrolyte decomposition layer may be minimized by tailoring the electrolyte composition based on mechanistic understanding of the anode–electrolyte interactions.

4. Conclusion

A self-aligned Cu–Si core–shell NW array has been designed and fabricated as a candidate anode material for Li-ion batteries. The amorphous silicon shell accommodates Li-ions and the copper core functions as a built-in current collector as well as a strong mechanical support. Initial half-cell testing has demonstrated high Coulombic efficiency (97–100% after the first cycle) and good capacity retention at a charge–discharge rate 2C or lower. However, the charge capacity decreased dramatically at high cycling rates (5C and 10C), caused in part by an electrolyte decomposition layer covering the NW array's top surface and restricting access of the electrolyte.

Acknowledgements

Research sponsored by the Laboratory Directed Research and Development Program of Oak Ridge National Laboratory. The characterization work was supported in part by ORNL's SHaRE User Facility, which is sponsored by the DOE Office of Basic Energy Sciences. This manuscript has been authored by UT-Battelle, LLC, under Contract No. DE-AC05-00OR22725 with the U.S. Department of Energy. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a non-exclusive, paid-up, irrevocable, world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for United States Government purposes.

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